Rec'd PCT/PTO 11 SEP 2000

FORM PTO-1390 (REV 5-93) — U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 951/49166

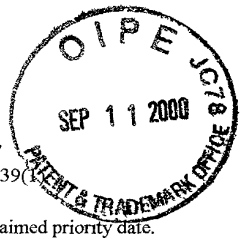
U.S. APPLICATION NO (if known, see 37 CFR 1.5): 09/646006

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EP99/01177	23 February 1999 (23-02-99)	10 March 1998 (10-03-98)

TITLE OF INVENTION: DATA BUS FOR A PLURALITY OF NODES

APPLICANT(S) FOR DO/EO/US: Martin PELLER

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:



1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371

3 [ ] This express request to begin national examination procedures (35 U.S.C. 371(f) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. [ ] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2)).

   a. [X] is transmitted herewith (required only if not transmitted by the International Bureau).

   b. [ ] has been transmitted by the International Bureau

   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US)

6. [ ] A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. [ ] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))

   a. [ ] are transmitted herewith (required only if not transmitted by the International Bureau).

   b. [ ] have been transmitted by the International Bureau.

   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.

   d. [ ] have not been made and will not be made.

8. [ ] A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)). (Unexecuted)

10. [ ] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S C. 371(c)(5)).

Item 11. to 16. below concern other document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included

13. [X] A FIRST preliminary amendment.

    [ ] A SECOND or SUBSEQUENT preliminary amendment.

14. [X] A substitute specification.

15. [ ] A change of power of attorney and/or address letter.

16. [X] Other items or information:

a. International Search Report
b. 1 Sheet Drawing showing Figure 1
c First page of Published Application

U S APPLICATION NO. (if known, see 37 CFR 1 5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/646006	PCT/EP99/01177	951/49166

17. [X] The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)):		
Search Report has been prepared by the EPO or JPO ..... $840.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) ..... $670.00 No international preliminary examination fee paid to USPTO (37 CFR 1.482)	840.00	
but international search fee paid to USPTO (37 CFR 1.445(a)(2) ..... $760.00 Neither international preliminary examination fee (37 CFR 1.482) nor		
international search fee (37CFR 1.445(a)(2) paid to USPTO ..... $ 970 00 International preliminary examination fee paid to USPTO (37 CFR 1.482)		
and all claims satisfied provisions of PCT Article 33(2)-(4) $96 00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$840.00	
Surcharge of $130.00 for furnishing the oath or declaration later than [ ] 20 [X] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$130.00	

Claims	Number Filed	Number Extra	Rate		
Total Claims	6-20=		X $18.00	$	
Independent Claims	2-3=		X $78.00	$	
Multiple dependent claims(s) (if applicable)			+ $260.00	$	
TOTAL OF ABOVE CALCULATIONS =				$970.00	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				$	
SUBTOTAL =				$970.00	
Processing fee of $130.00 for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$970.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28,3.31). $40.00 per property +				$	
TOTAL FEE ENCLOSED =				$970.00	
				Amount to be: refunded	$
				charged	$

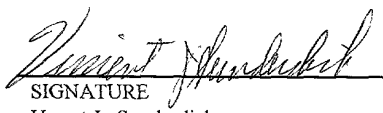
a. [X] One check in the amount of $970.00 for the filing fee is enclosed

b. [ ] Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees, which may be required, or credit any overpayment to Deposit Account No. 05-1323 . A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1 137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:
Evenson, McKeown, Edwards & Lenahan, P.L.L C.
1200 G Street, N.W., Suite 700
Washington, D.C. 20005
Tel. No. (202) 628-8800
Fax No. (202) 628-8844



SIGNATURE
Vicent J. Sunderdick
NAME
29,004
REGISTRATION NUMBER
September 11, 2000
DATE

Attorney Docket: 951/49166
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: MARTIN PELLER

Serial No.: NOT YET ASSIGNED PCT NO. PCT/EP99/01177

Filed: September 11, 2000

Title: DATA BUS FOR A PLURALITY OF NODES

PRELIMINARY AMENDMENT

Box PCT APPLICATION
Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified application as follows:

IN THE SPECIFICATION:

A substitute specification is submitted herewith.

IN THE CLAIMS:

Cancel Claims 1-4 and add new claims 5-10 as follows:

--5. A data bus for a plurality of nodes which exchange data with one another over at least one electrical line, said data bus comprising:

a plurality of data exchange module each having a first input for receiving input data from respective ones of said plurality of nodes and providing a corresponding electrical output signal;

a logic decision gate having a plurality of inputs with each input receiving said respective electrical output signal wherein a single output of said decision gate is connected to a second input of each of said plurality data exchange modules.

6. The data bus according to Claim 5, wherein each of said data exchanges comprises an opto-electrical transducer wherein an output of said nodes is connected through an optical transmission element to said opto-electronic transducer.

7. The data bus according according to Claim 5, further comprising a signal preparation circuit positioned between said logic decision gate and said second input of said data exchange wherein said signal preparation circuit includes means for adjusting the output signal to a pulse form.

8. The data bus according to Claim 5, further comprising additional logic decision gates positioned between an output of said signal preparation circuit and one of said nodes.

9. An improved method of exchanging data among a plurality of nodes, comprising the steps of:

providing a logical decision gate having a plurality of inputs corresponding to the number of plurality of nodes;

outputting information from each of said plurality of nodes;

converting said information into perspective electrical outputs;

providing said electrical outputs to said inputs of said logical decision gate; and providing an output of said logical decision gate transforming said output and providing said transformed output to an input of each of said nodes.

10. The method according to Claim 9, including the further step of providing a signal preparation circuit between said logic decision gate output and said plurality of nodes in order to provide a pulse formation adjustment of said output signal. --

IN THE ABSTRACT:

Please add an Abstract of the Disclosure submitted herewith on a separate page.

REMARKS

No new matter is added by the above amendment and applicant therefore request a full and thorough examination on the merits of this application containing Claim 5-10.

Entry of the amendments to the specification, claims and abstract before examination of the application is respectfully requested.

If there are any questions regarding this Preliminary Amendment or this application in general, a telephone call to the

undersigned would be appreciated since this should expedite the prosecution of the application for all concerned.

It is respectfully requested that, if necessary to effect a timely response, this paper be considered as a Petition for an Extension of Time sufficient to effect a timely response and shortages in other fees, be charged, or any overpayment in fees be credited, to the Account of Evenson, McKeown, Edwards & Lenahan, P.L.L.C., Deposit Account No. 05-1323 (Docket #)951/49166.

Respectfully submitted,

September 11, 2000

Vincent J. Sunderdick
Registration No. 29,004

VJS/rrt

EVENSON, McKEOWN, EDWARDS
& LENAHAN
1200 G Street, N.W., Suite 700
Washington, DC 20005
Telephone No.: (202) 628-8800
Facsimile No.: (202) 628-8844

-- **ABSTRACT OF THE DISCLOSURE**

An arrangement for exchanging data among a plurality of nodes by providing a logical decision gate wherein inputs of the logical decision gate are providing with converted node output signal and wherein the output of the logical decision gate provides signals to each of said nodes through a respective signal converter. The signal converter outputs electrical signals to said logical decision gate. --

Attorney Docket: 951/49166
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: MARTIN PELLER

Serial No.: NOT YET ASSIGNED PCT No. PCT/EP99/01177

Filed: September 11, 2000

Title: DATA BUS FOR A PLURALITY OF NODES

SUBMISSION OF SUBSTITUTE SPECIFICATION

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Attached is a Substitute Specification and a marked-up copy of the original specification. I certify that said substitute specification contains no new matter and includes the changes indicated in the marked-up copy of the original specification.

Respectfully submitted,

September 11, 2000

Vincent J. Sunderdick
Registration No. 29,004

EVENSON, McKEOWN, EDWARDS
& LENAHAN, P.L.L.C.
1200 G Street, N.W., Suite 700
Washington, DC 20005
Telephone No.: (202) 628-8800
Facsimile No.: (202) 628-8844

VJS/rrt

TITLE OF THE INVENTION

Data Bus for a Plurality of Nodes

This application claims the priority of German Patent Application 198 10 294.1, filed August 10, 1998 and PCT/EP99/01177 filed February 23, 1999, the disclosures of which are expressly incorporated by reference herein.

The invention relates to a star-shaped data bus for a plurality of nodes which exchange data with one another over at least one electric line. The circuit-technological realization of a data bus of this type is known in the form of an open collector circuit. An open collector circuit has the disadvantage that at high rates of transmission and many bus nodes a relatively small resistance value must be used as collector resistance in order to achieve a sufficient steepness of the edge of the signal information present in pulse form. This leads to high currents and the necessity of use of power transistors and power resistors as well as high power losses.

The objective of the invention is to provide a data bus of the type stated initially which makes possible interference-free bus communication with low circuit-technological expenditure even in the case of a large number of bus nodes.

The central element of the data bus according to the invention is the logical decision gate having inputs for receiving the signal outputs of the bus nodes. The logical decision gate requires for no expensive signal form processing devices. It transmits the signals unchanged in their form. Also the required power consumption is low even in the case of a large number of nodes.

The invention may be used with nodes which supply electrical output information as well as with nodes which generate optical output signals. The optical nodes are connected via opto-electric transducers on the data bus so that the signal outputs of the nodes, via each transducer of this type, are fed to the logical decision gate and the output of the logical decision gate is fed, via a common electric-optical transducer or else via individual transducers of this type, to the inputs of the nodes.

For a data bus which is configured as an open collector circuit it is known to provide signal form processing devices (cf. US 5,684,831). Therein a device of this type is provided for each node. The configuration according to the invention for the data bus with a logical decision gate now permits reducing the circuit-technological expenditure drastically. It is only

necessary to connect a single signal preparation circuit between the logical decision gate and the inputs of the nodes. This signal preparation circuit models the output signal of the logical decision gate with regard to pulse form. This can be accomplished with an adjustment of the form of the output signal to the form of the input signals or by an adaptation as is described in US 5,684,831. According to this method, the leading edges are flattened in order to be able to distinguish the usable signal from high-frequency interference signals with extreme edge steepness.

Finally, additional embodiments of the invention use additional logical decision gates which can be disposed between the output of the signal preparation circuit and at least one of the nodes. It is when possible to separate certain sections of the data bus, as needed, in order, for example, to separate a faultily functioning bus node or else to set several bus nodes into Sleep mode.

Other objects, advantages and novel features of the present invention will become apparent from the following detailed description of the invention when considered in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The single figure shows schematically the layout of the data bus according to the invention which achieves reliable bus communication for a plurality of bus nodes with low circuit-technological expenditure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A data bus serves to connect the nodes to one another which supply optical information. The output of the nodes (for the sake of comprehensibility two nodes T_n and T_{n+1} are indicated) are fed to inputs of opto-electric signal transducers S/E_n and S/E_{n+1} as input signals. The electric signals (Di_n, Di_{n+1}) output from these transducers are linked with an AND gate 1. The number of the input and outputs of the gate corresponds to the number of the bus nodes. The output 2 of the AND gate 1 drives all the inputs (Do_n, Do_{n+1}) of the transducers S/E_n and S/E_{n+1} which supply optical signals in the form of a pulse to the nodes via optical transmission segments.

In this manner each node receives all the information are issued by the other nodes as well as its own information.

The AND gate 1 has a significantly lower power consumption than the open collector circuit mentioned initially.

A signal preparation device SA at the output of the AND gate 1 eliminates, distortions of signal form, such as can arise through opto-electrical transducers (S/E_n and S/E_{n+1}). For example, NRZ (non-return-to-zero) -coded signals which experience a distortion of up to 30% signal length through the transducer S/E can be brought into a form without pulse distortion.

For the signal preparation in the device SA, for example, the same sampling process can be used which is used for the individual nodes. It is also possible to use a special signal preparation process which takes into account the special auxiliary conditions in the data bus. Thereby data transmission is significantly more robust. It is possible to filter out brief glitches. The demands on the sampling process in the individual nodes can be set lower or the tolerance with respect to pulse distortion grows on one transmission segment. The sampling process is clearly less susceptible to quartz jitter. For the same robustness quartzes with lower frequency and less cost can be used.

The foregoing disclosure has been set forth merely to illustrate the invention and is not intended to be limiting. Since modifications of the disclosed embodiments incorporating the spirit and substance of the invention may occur to persons skilled in the art, the invention should be construed to include everything within the scope of the appended claims and equivalents thereof.

Claims

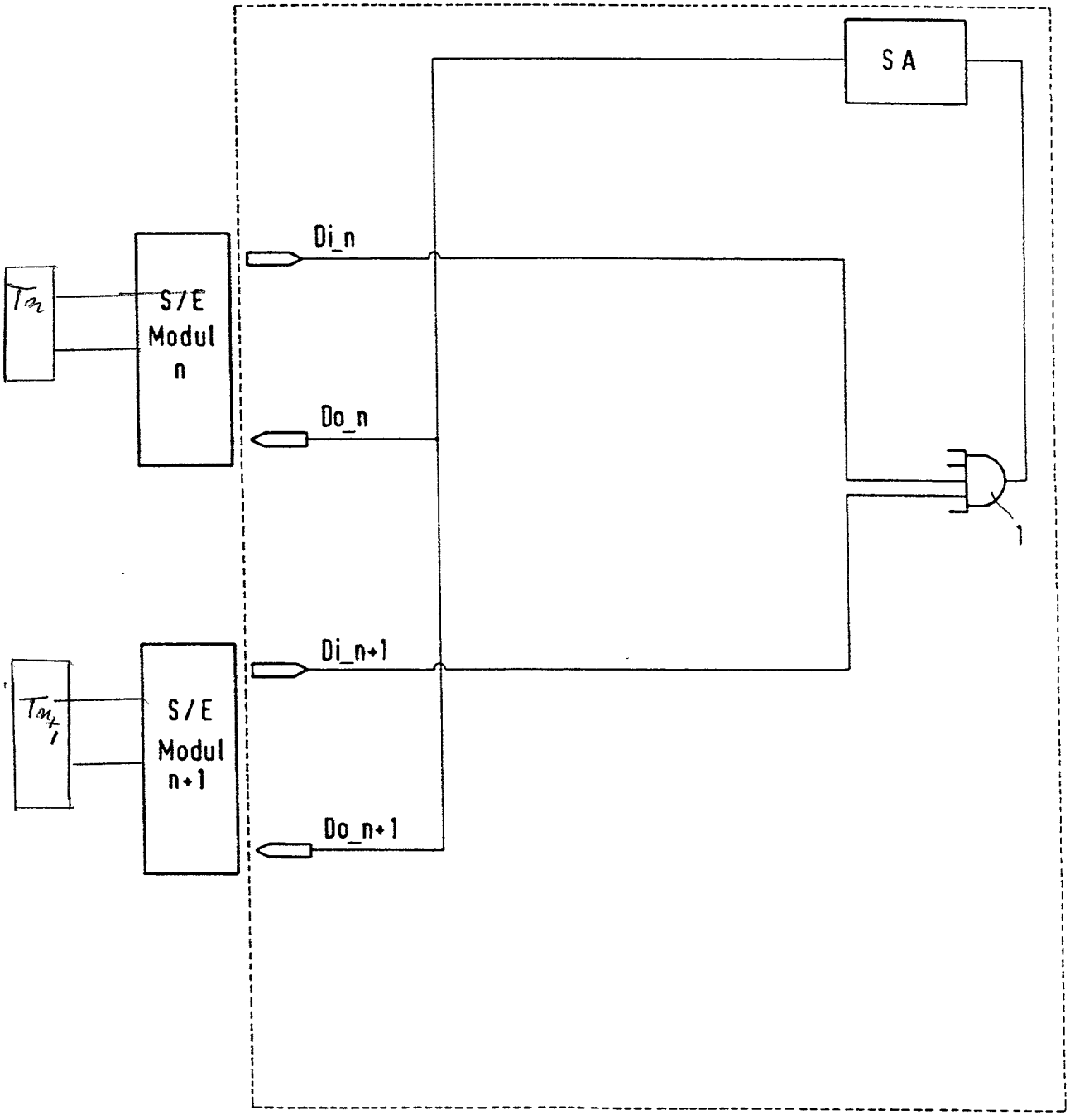
1. Data bus for a plurality of nodes which exchange data telegrams with one another over at least one electric line characterized by the fact that the input signals of the star coupler are present in electrical form, that the star coupler contains a logical decision gate to whose inputs the outputs of the nodes are connected and to which the input signals are fed, and that the output of the decision gate is connected to the inputs of the nodes in a parallel manner.

2. Data bus according to Claim 1 characterized by the fact that at least one part of the nodes is connected via an optical transmission segment to opto-electrical transducers on the star coupler which are connected on the load side or on the line side.

3. Data bus according to Claim 1 or 2 characterized by the fact that a signal preparation circuit is disposed between the logical decision gate and the inputs of the nodes, said signal preparation circuit adjusting the output signal to the input signal with regard to pulse form.

4. Data bus according to one of the Claims 1 to 3 characterized by the fact that additional logical decision gates are disposed between the output of the signal preparation circuit and at least one part of the nodes.

Modul = module


SA
Di_n
Tn
S/E
Modul
n
Do_n
1
Di_n+1
Tn+1
S/E
Modul
n+1
Do_n+1

TITLE OF THE INVENTION

Data Bus for a Plurality of Nodes

This application claims the priority of German Patent Application 198 10 294.1, filed August 10, 1998 and PCT/EP99/01177 filed February 23, 1999, the disclosures of which are expressly incorporated by reference herein.

The invention relates to a star-shaped data bus for a plurality of nodes which exchange data [telegrams] with one another over at least one electric line. The circuit-technological realization of a data bus of this type is known in the form of an open collector circuit. An open collector circuit has the disadvantage that at high rates of transmission and many bus nodes a relatively small resistance value must be used as collector resistance in order to achieve a sufficient steepness of the edge of the signal [telegrams] information present in pulse form. This leads to high currents and the necessity of use of power transistors and power resistors as well as high power losses [of power which are too high].

The objective of the invention is to provide a data bus of the type stated initially which makes possible interference-free bus communication with low circuit-technological expenditure even in the case of a large number of bus nodes.

[The invention realizes this objective with the characteristics of Claim 1.]

The central element of the data bus according to the invention is the logical decision gate [to whose] having inputs for receiving the signal outputs of the bus nodes [are fed]. The logical decision gate requires for [its use] no expensive signal form processing devices. It transmits the signals unchanged in their form. Also the required power consumption is low even in the case of a large number of nodes.

[Developments of the] The invention [are possible] may be used with nodes which supply electrical output [telegrams] information as well as with nodes which generate optical output signals. The [latter] optical nodes are connected via opto-electric transducers [in such a way] on the data bus so that the signal outputs of the nodes, via each transducer of this type, are fed to the logical decision gate and the output of the logical decision gate is fed, via a common electric-optical transducer or else via individual transducers of this type, to the inputs of the nodes.

For a data bus which is configured as an open collector circuit it is [prior art] known to provide signal form processing devices (cf. US 5,684,831). Therein a device of this type is provided for each node. The configuration

according to the invention for the data bus with a logical decision gate now permits reducing the circuit-technological expenditure drastically. It is only [still required to dispose] necessary to connect a single signal preparation circuit between the logical decision gate and the inputs of the nodes, [, said] This signal preparation circuit [modeling] models the output signal of the logical decision gate with regard to pulse form. This can be accomplished with an adjustment of the form of the output signal to the form of the input signals or [else also] by an adaptation as is described in US 5,684,831[A]. [Therein] According to this method, the leading edges are flattened in order to be able to distinguish the usable signal from high-frequency interference signals with extreme edge steepness [of edge].

Finally, [in the case of] additional [forms of embodiment] embodiments of the invention[,] use additional logical decision gates which can be disposed between the output of the signal preparation circuit and at least one [part] of the nodes. [Thereby it] It is when possible to separate certain sections of the data bus, as needed, in order, for example, to separate a faultily functioning bus node or else to set several bus nodes into Sleep mode.

Other objects, advantages and novel features of the present invention will become apparent from the following detailed

description of the invention when considered in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[With the aid of the drawing, the invention will be explained in more detail.]

The single figure shows schematically the layout of the data bus according to the invention which achieves reliable bus communication for a plurality of bus nodes with low circuit-technological expenditure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A data bus [shown in extract] serves to connect the nodes to one another which supply optical [telegrams] information. The [telegrams] output of the nodes (for the sake of comprehensibility two nodes T_n and T_{n+1} are indicated) are fed to inputs of opto-electric signal transducers S/E_n and S/E_{n+1} as input signals. The electric signals (Di_n, Di_{n+1}) output from [of] these transducers are linked with an AND gate 1. The number of the input and outputs of the gate corresponds to the number of the bus nodes. The output 2 of the AND gate 1 drives all the inputs (Do_n, Do_{n+1}) of the transducers S/E_n and S/E_{n+1}[. [These] which supply optical signals in the form of a pulse [which supply these telegrams] to the nodes via optical transmission segments [not represented].

In this manner each node receives all the [telegrams which] information are issued by the other nodes as well as its own [telegram] information.

[As already stated, the] The AND gate 1 has a significantly lower power consumption than the open collector circuit mentioned initially.

[Also shown is the use of a] A signal preparation device SA at the output of the AND gate 1[. Thereby, for example,] eliminates, distortions of signal form, such as can arise through opto-electrical transducers (S/E_n and S/E_{n+1})[, can be eliminated]. For example, NRZ (non-return-to-zero) -coded signals which experience a distortion of up to 30% signal length through the transducer S/E can be brought into a form without pulse distortion.

For the signal preparation in the device SA, for example, the same sampling process can be used which is used for the individual nodes. It is also possible to use a special signal preparation process which takes into account the special auxiliary conditions in the data bus. Thereby data transmission is significantly more robust. It is possible to filter out brief glitches. The demands on the sampling process in the individual nodes can be set lower or the tolerance with respect to pulse distortion grows on one transmission segment.

The sampling process is clearly less susceptible to quartz jitter. For the same robustness quartzes with lower frequency <u>and less cost</u> can be used [whereby cost advantages follow].

The foregoing disclosure has been set forth merely to illustrate the invention and is not intended to be limiting. Since modifications of the disclosed embodiments incorporating the spirit and substance of the invention may occur to persons skilled in the art, the invention should be construed to include everything within the scope of the appended claims and equivalents thereof.

Data Bus for a Plurality of Nodes

Claims

1. Data bus for a plurality of nodes which exchange data telegrams with one another over at least one electric line characterized by the fact that the input signals of the star coupler are present in electrical form, that the star coupler contains a logical decision gate to whose inputs the outputs of the nodes are connected and to which the input signals are fed, and that the output of the decision gate is connected to the inputs of the nodes in a parallel manner.

2. Data bus according to Claim 1 characterized by the fact that at least one part of the nodes is connected via an optical transmission segment to opto-electrical transducers on the star coupler which are connected on the load side or on the line side.

3. Data bus according to Claim 1 or 2 characterized by the fact that a signal preparation circuit is disposed between the logical decision gate and the inputs of the nodes, said signal preparation circuit adjusting the output signal to the input signal with regard to pulse form.

4. Data bus according to one of the Claims 1 to 3 characterized by the fact that additional logical decision gates are disposed between the output of the signal preparation circuit and at least one part of the nodes.

1/1

[figure]

Modul = module

(English Translation)
WO 99/46898

Data Bus for a Plurality of Nodes

The invention relates to a star-shaped data bus for a plurality of nodes which exchange data telegrams with one another over at least one electric line. The circuit-technological realization of a data bus of this type is known in the form of an open collector circuit. An open collector circuit has the disadvantage that at high rates of transmission and many bus nodes a relatively small resistance value must be used as collector resistance in order to achieve a sufficient steepness of the edge of the signal telegrams present in pulse form. This leads to high currents and the necessity of use of power transistors and power resistors as well as losses of power which are too high.

The objective of the invention is to provide a data bus of the type stated initially which makes possible interference-free bus communication with low circuit-technological expenditure even in the case of a large number of bus nodes.

The invention realizes this objective with the characteristics of Claim 1.

The central element of the data bus according to the invention is the logical decision gate to whose inputs the signal outputs of the bus nodes are fed. The logical decision gate

requires for its use no expensive signal form processing devices. It transmits the signals unchanged in their form. Also the required power consumption is low even in the case of a large number of nodes.

Developments of the invention are possible with nodes which supply electrical output telegrams as well as with nodes which generate optical output signals. The latter nodes are connected via opto-electric transducers in such a way on the data bus the signal outputs of the nodes via each transducer of this type are fed to the logical decision gate and the output of the logical decision gate is fed via a common electric-optical transducer or else via individual transducers of this type to the inputs of the nodes.

For a data bus which is configured as an open collector circuit it is prior art to provide signal form processing devices (cf. US 5,684,831). Therein a device of this type is provided for each node. The configuration according to the invention for the data bus with a logical decision gate now permits reducing the circuit-technological expenditure drastically. It is only still required to dispose a single signal preparation circuit between the logical decision gate and the inputs of the nodes, said signal preparation circuit modeling the output signal of the logical decision gate with regard to pulse form.

This can be an adjustment of the form of the output signal to the form of the input signals or else also an adaptation as is described in US 5,684,831 A. Therein the leading edges are flattened in order to be able to distinguish the usable signal from high-frequency interference signals with extreme steepness of edge.

Finally, in the case of additional forms of embodiment of the invention, additional logical decision gates can be disposed between the output of the signal preparation circuit and at least one part of the nodes. Thereby it is possible to separate certain sections of the data bus as needed in order, for example, to separate a faultily functioning bus node or else to set several bus nodes into Sleep mode.

With the aid of the drawing, the invention will be explained in more detail. The single figure shows schematically the layout of the data bus according to the invention which achieves reliable bus communication for a plurality of bus nodes with low circuit-technological expenditure.

A data bus shown in extract serves to connect the nodes to one another which supply optical telegrams. The telegrams of the nodes (for the sake of comprehensibility two nodes T_n and T_{n+1} are indicated) are fed to inputs of opto-electric signal

transducers S/E_n and S/E_{n+1} as input signals. The electric signals (Di_n, Di_{n+1}) of these transducers are linked with an AND gate 1. The number of the input and outputs of the gate corresponds to the number of the bus nodes. The output 2 of the AND gate 1 drives all the inputs (Do_n, Do_{n+1}) of the transducers S/E_n and S/E_{n+1}. These supply optical signals in the form of a pulse which supply these telegrams to the nodes via optical transmission segments not represented.

In this manner each node receives all the telegrams which are issued by the other nodes as well as its own telegram.

As already stated, the AND gate 1 has a significantly lower power consumption than the open collector circuit mentioned initially.

Also shown is the use of a signal preparation device SA at the output of the AND gate 1. Thereby, for example, distortions of signal form, such as can arise through opto-electrical transducers (S/E_n and S/E_{n+1}), can be eliminated. For example, NRZ (non-return-to-zero) -coded signals which experience a distortion of up to 30% signal length through the transducer S/E can be brought into a form without pulse distortion.

For the signal preparation in the device SA, for example, the same sampling process can be used which is used for the

individual nodes. It is also possible to use a special signal preparation process which takes into account the special auxiliary conditions in the data bus. Thereby data transmission is significantly more robust. It is possible to filter out brief glitches. The demands on the sampling process in the individual nodes can be set lower or the tolerance with respect to pulse distortion grows on one transmission segment. The sampling process is clearly less susceptible to quartz jitter. For the same robustness quartzes with lower frequency can be used whereby cost advantages follow.

Data Bus for a Plurality of Nodes

Claims

1. Data bus for a plurality of nodes which exchange data telegrams with one another over at least one electric line characterized by the fact that the input signals of the star coupler are present in electrical form, that the star coupler contains a logical decision gate to whose inputs the outputs of the nodes are connected and to which the input signals are fed, and that the output of the decision gate is connected to the inputs of the nodes in a parallel manner.

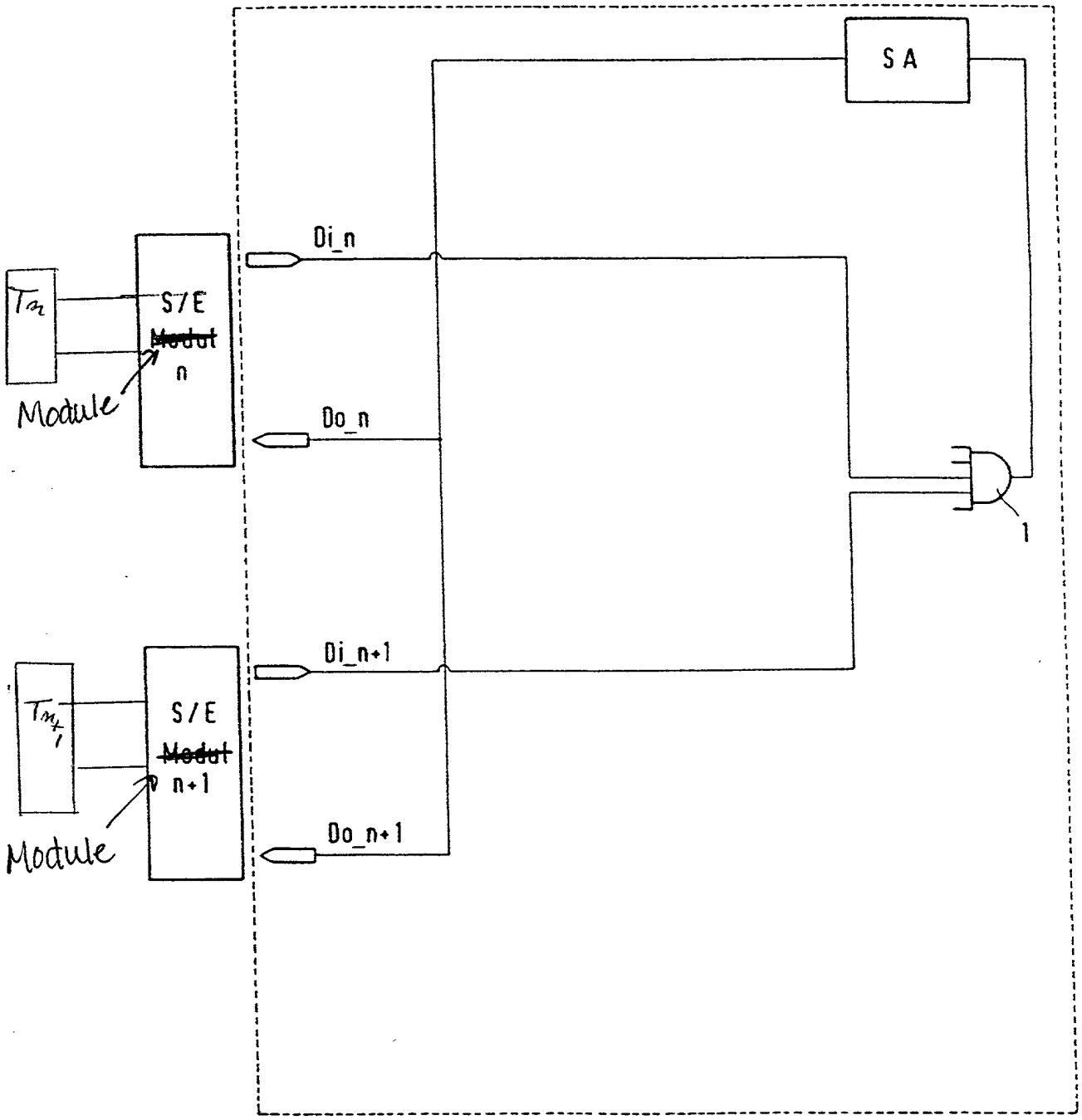
2. Data bus according to Claim 1 characterized by the fact that at least one part of the nodes is connected via an optical transmission segment to opto-electrical transducers on the star coupler which are connected on the load side or on the line side.

3. Data bus according to Claim 1 or 2 characterized by the fact that a signal preparation circuit is disposed between the logical decision gate and the inputs of the nodes, said signal preparation circuit adjusting the output signal to the input signal with regard to pulse form.

4. Data bus according to one of the Claims 1 to 3 characterized by the fact that additional logical decision gates are disposed between the output of the signal preparation circuit and at least one part of the nodes.

[figure]

Modul = module


SA
Di_n
Tx
S/E
Modul
n
Module
Do_n
1
Di_n+1
Tx+1
S/E
Modul
n+1
Module
Do_n+1

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (includes Reference to PCT International Applications)	ATTORNEY'S DOCKET NUMBER 951/49166

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Data Bus For A Plurality of Nodes

the specification of which (check only one item below):

[ ] is attached hereto.

[ ] was filed as United States application
Serial No. _____
on _____
and was amended
on _____ (if applicable).

[X] was filed as PCT international application
Number PCT/EP99/01177
on February 23, 1999
and was amended under PCT Article 19
on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations. §1.56(a).

I hereby claim foreign priority benefits under Title 35, United State Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

COUNTRY (if PCT indicate PCT)	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
Germany	198 10 294.1	10 March 1998	[X] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No

Combined Declaration For Patent Application and Power of Attorney (Continued) (includes Reference to PCT international Applications	ATTORNEY'S DOCKET NUMBER 951/49166

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application(s) and the national of PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120

U.S. APPLICATIONS		STATUS *(Check one)*		
U.S. APPLICATION NUMBER	U.S. FILING DATE	PATENTED	PENDING	ABANDONED

PCT APPLICATIONS DESIGNATING THE U.S.					
PCT APPLICATION NO	PCT FILING DATE	U.S. SERIAL NUMBERS ASSIGNED (IF ANY)			

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (List name and registration number)

8 — Martin Fleit, Reg. No. 16,900; Herbert I. Cantor, Reg. No. 24,392; James F. McKeown, Reg. No. 25,406; Donald D. Evenson, Reg. No. 26,160; Joseph D. Evans, Reg. No. 26,269; Gary R. Edwards, Reg. No. 31,824; Jeffrey D. Sanok, Reg. No. 32,169; and Richard R. Diefendorf, Reg. No. 32,390

Send Correspondence to:	Direct Telephone Calls to: *(name and telephone number)*
Evenson, McKeown, Edwards & Lenahan, P.L.L.C. 1200 G Street, N.W., Suite 700 Washington, D.C. 20005	(202) 628-8800

201	FULL NAME OF INVENTOR	FAMILY NAME **PELLER**	FIRST GIVEN NAME **Martin**	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY Muenchen	STATE OR FOREIGN COUNTRY DEX	COUNTRY OF CITIZENSHIP Germany
	POST OFFICE ADDRESS	POST OFFICE ADDRESS Adelheidstr. 38	CITY Muenchen	STATE & ZIP CODE/COUNTRY D-80796, Germany
202	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY
203	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true: and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201	SIGNATURE OF INVENTOR 202	SIGNATURE OF INVENTOR 203
Martin Peller		
DATE 08/28/2000	Date	DATE